Claims

1. An apparatus for generating a supply voltage internally within an integrated circuit comprising:

a charge pump stage structure having a pumping capacitor connected to a pumping node, a first PMOS device connected to an input node, said first PMOS device configured to electrically communicate with said pumping capacitor, wherein said first PMOS device is configured to connect said pumping node to said input node when said pumping capacitor is not boosted;

a second PMOS device connected to an output node, said second PMOS device configured to electrically communicate with said pumping capacitor, said second PMOS device configured to transfer electrical charge from said pumping node to said output node when said pumping capacitor is boosted, said second PMOS device configured to prevent a reversal current feedback from said output node to said pumping node when said pumping capacitor is not boosted; and

a third PMOS device configured to electrically communicate with said first PMOS device, wherein said third PMOS device is configured to connect said pumping node to a gate of said second PMOS device to prevent said current feedback.

2. The apparatus of claim 1, wherein said third PMOS device is configured to connect the pump node to a gate of said second device in order to prevent said current feedback from said pumping node to said input node when said pumping capacitor is boosted.

3. The apparatus of claim 1 further including:

an auxiliary capacitor connected to said first PMOS device, wherein said auxiliary capacitor is configured to generate an undershoot on said gate of said first PMOS device, and wherein said auxiliary capacitor is configured to switch said apparatus to an "ON" state when an electrical current is transferred from said input node to said pumping node.

4. An apparatus for generating a supply voltage internally within an integrated circuit comprising:

a symmetrical charge pump stage structure comprising a first substructure and a second substructure, each said substructure having a pumping capacitor connected to a pumping node, a first PMOS device connected to an input node, said first PMOS device configured to electrically communicate with said coupling capacitor; wherein said first PMOS device is configured to connect said pumping node to said input node when said pumping capacitor is not boosted;

a second PMOS device connected to an output node, said second PMOS device configured to electrically communicate with said pumping capacitor, said second PMOS device configured to transfer electrical charge from said pumping node to said output node when said pumping capacitor is boosted, said second PMOS device configured to prevent a reversal current feedback from said output node to said pumping node when said pumping capacitor is not boosted; and

a third PMOS device configured to electrically communicate with said first PMOS device, wherein said third PMOS device is configured to connect said pumping

node to a gate of said second device to prevent a reversal current feedback from said pumping node to said input node when said pumping capacitor is boosted.

5. The apparatus of claim 4, wherein said third PMOS device is configured to switch a gate of said first PMOS device to a boosted pump node potential in order to prevent said current feedback from said pumping node to said input node when said pumping capacitor is boosted.

6. The apparatus of claim 4, wherein each said substructure further comprises:

an auxiliary capacitor connected to said first PMOS device, wherein said auxiliary capacitor is configured to generate an undershoot on said gate of said first PMOS device, and wherein said auxiliary capacitor is configured to switch said apparatus to an "ON" state when an electrical current is transferred from said input node to said pumping node.

7. An apparatus for generating a supply voltage internally within an integrated circuit comprising:

an independently controlled charge pump stage having an input control node, a pumping capacitor connected to a pumping node, a first PMOS device connected to said input control node, said first PMOS device configured to electrically communicate with said coupling capacitor, wherein said first PMOS device is configured to connect said pumping node to said input control node when said pumping capacitor is not boosted;

a second PMOS device connected to an output control node, said second PMOS device configured to electrically communicate with said pumping capacitor, said second PMOS device configured to transfer electrical charge from said pumping node to said output control node when said pumping capacitor is boosted, said second PMOS device configured to prevent a reversal current feedback from said output control node to said pumping node when said pumping capacitor is not boosted; and

a third PMOS device electrically communicating with said first PMOS device, wherein said third PMOS device is configured to connect said pumping node to a gate of said second device to prevent a reversal current feedback from said pumping node to said input control node when said pumping capacitor is boosted.

8. The apparatus of claim 7, wherein said third PMOS device is configured to switch a gate of said first PMOS device to a boosted pump node potential in order to prevent said current feedback from said pumping node to said input control node when said pumping capacitor is boosted.

9. The apparatus of claim 7, wherein each said substructure further comprises:

an auxiliary capacitor connected to said first PMOS device, wherein said auxiliary capacitor is configured to generate an undershoot on said gate of said first PMOS device, and wherein said auxiliary capacitor is configured to switch said apparatus to an "ON" state when an electrical current is transferred from said input control node to said pumping node.

10. An apparatus for generating a supply voltage internally within an integrated circuit comprising:

an independently controlled symmetrical charge pump stage structure comprising a first independently controlled substructure and a second independently controlled substructure, each said independently controlled substructure having:

an input control node;

a pumping capacitor connected to a pumping node;

a first PMOS device connected to said input control node, said first PMOS device configured to electrically communicate with said coupling capacitor, wherein said first PMOS device is configured to connect said pumping node to said input control node when said pumping capacitor is not boosted;

a second PMOS device connected to an output control node; said second PMOS device configured to electrically communicate with said pumping capacitor, said second PMOS device configured to transfer electrical current from said pumping node to said output control node when said pumping capacitor is boosted, said second PMOS device configured to prevent a reversal current feedback from said output control node to said pumping node when said pumping capacitor is not boosted; and

a third PMOS device configured to electrically communicate with said first PMOS device, wherein said third PMOS device is configured to connect said pumping node to a gate of said second device to prevent a reversal current feedback from said pumping node to said input control node when said pumping capacitor is boosted.

11. The apparatus of claim 10, wherein said third PMOS device is configured to switch a gate of said first PMOS device to a boosted pump node potential in order to prevent said current feedback from said pumping node to said input control node when said pumping capacitor is boosted.

12. The apparatus of claim 10, wherein each said independently controlled substructure further comprises:

an auxiliary capacitor connected to said first PMOS device, wherein said auxiliary capacitor is configured to generate an undershoot on said gate of said first PMOS device, and wherein said auxiliary capacitor is configured to switch said apparatus to an "ON" state when an electrical current is transferred from said input control node to said pumping node.

13. An apparatus for generating a supply voltage internally within an integrated circuit comprising:

a plurality of symmetrical charge pump stages cascade-connected in series having:

a first symmetrical pump charge stage connected to an input node; and

a last symmetrical pump charge stage connected to an output node.

14. The apparatus of claim 13 further comprising;

at least one intermediate symmetrical pump charge stage therebetween.

15. The apparatus of claim 13, wherein each said symmetrical pump charge stage further comprises a first substructure and a second substructure, each said substructure further comprising:

a pumping capacitor connected to a pumping node;

a first PMOS device connected to an input node, said first PMOS device configured to electrically communicate with said coupling capacitor, wherein said first PMOS device is configured to connect said pumping node to said input node when said pumping capacitor is not boosted;

a second PMOS device connected to an output node; said second PMOS device configured to electrically communicate with said pumping capacitor, said second PMOS device configured to transfer electrical charge from said pumping node to said output node when said pumping capacitor is boosted, said second PMOS device configured to prevent a reversal current feedback from said output node to said pumping node when said pumping capacitor is not boosted; and

a third PMOS device configured to electrically communicate with said first PMOS device, wherein said third PMOS device is configured to connect said pumping node to a gate of said second device to prevent a reversal current feedback from said pumping node to said input node when said pumping capacitor is boosted.

16. An apparatus for generating a supply voltage internally within an integrated circuit comprising:

a symmetrical pump charge stage connected to an input node; and

a plurality of independently controlled symmetrical charge pump stages cascade-connected in series comprising:

a first independently controlled symmetrical pump charge stage connected to said symmetrical pump charge stage; and

a last independently controlled symmetrical pump charge stage connected to an output node.

17. The apparatus of claim 16 further comprising:

at least one intermediate independently controlled symmetrical pump charge stage therebetween.

18. The apparatus of claim 16, wherein each said independently controlled symmetrical charge pump stage further comprises a first independently controlled substructure and a second independently controlled substructure, each said independently controlled substructure having:

an input control node;

a pumping capacitor connected to a pumping node;

a first PMOS device connected to said input control node, said first PMOS device configured to electrically communicate with said coupling capacitor, wherein said first PMOS device is configured to connect said pumping node to said input control node when said pumping capacitor is not boosted;

a second PMOS device connected to an output control node, said second PMOS device configured to electrically communicate with said pumping capacitor, said second PMOS device configured to transfer electrical current from said pumping node to said output control node when said pumping capacitor is boosted, said second PMOS device configured to prevent a reversal current feedback from said output control node to said pumping node when said pumping capacitor is not boosted; and

a third PMOS device configured to electrically communicate with said first PMOS device, wherein said third PMOS device is configured to connect said pumping node to a gate of said second device to prevent a reversal current feedback from said pumping node to said input control node when said pumping capacitor is boosted.